Investigation of FECTED Performance for Millimeter-Wave Applications

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***Abstract*—The potential of GaAs, $Ga_{0.47}In_{0.53}As$, and InP field-effect cathode transferred-electron device (FECTED) oscillators is theoretically investigated at millimeter wave. The modeling relies on a general time-domain electronic circuit simulator including a quasi-two-dimensinal bipolar hydrodynamic FECTED model. Pure sine simulations have been performed to optimize the device structure and performance at various typical frequencies in a self-consistent manner, together with thermal and electronic limitations. The optimization is focused on a reliable and high negative resistance level device based on a dipolar-layer single transit mode. By means of transient simulations, we next demonstrate the feasibility of simple front-end FECTED circuits for short-range pulsed and frequency-modulation continuous-wave millimeter-wave radars.**

***Index Terms*—Circuit simulation, FECTED oscillator, millimeter-wave application, radar front-end, semiconductor device physical modeling.**

I. Introduction

THE main application of the field-effect cathode transferred-electron device (FECTED) is the realization of millimeter-wave oscillators. Let us just recall that the FECTED structure is similar to that of a MESFET (see Fig. 1). In this structure, the gate Schottky contact plays a basic role since it determines the operating mode of the device. Indeed, the reverse gate–source voltage allows to control the dc current injected in the active zone. Two main operating modes were identified depending on the relative values of the gate–source and drain–source voltages [1], [2]. When the dc current is lower than what we called the valley current, the operating mode is a nontransit-time limited mode, where no Gunn domain transits in the device (FET mode). This mode has been theoretically investigated and experimentally demonstrated, mainly by Thim *et al.* [3], [4], where great technological work has been performed, yielding attractive experimental results up to 60 GHz [5], [6]. Thus, the validity of the concept and the feasibility of millimeter-wave applications are no longer demonstrated. However, in this operating mode, the active zone of the channel includes a positive resistance contributing to loss, as described previously in [2] and [4]. On the contrary, when the dc current is close to the valley current, a dipolar-layer transit mode occurs. The latter appears itself to be quite attractive and theoretically yields higher output power levels than the FET mode since this loss resistance does not exist any longer in this transit-time mode. The device can be designed to operate in an efficient overlength dipolar-layer mode inducing a more or less uniform electric-field distribution throughout the entire active zone of the device [2]. It can also be designed to operate in a single dipolar-layer transit mode. To our knowledge, this operating mode has not been exhaustively studied as yet. Thus, it appears interesting to add to the amount of work already achieved for the FET mode by performing a complementary study. Obviously, the theoretical results presented in this paper cannot be directly compared to the experimental results achieved by Thim *et al.* since they do not account for the same operating conditions. However, the ensemble is quite coherent and complementary.

In this context, the first part of this paper reports on the potential of GaAs, $Ga_{0.47}In_{0.53}As$, and InP FECTED oscillators at millimeter waves. The modeling relies on a general time-domain electronic circuit simulator including a quasi-bidimensional (Q-2-D) bipolar hydrodynamic FECTED model. Pure sine simulations have been performed to optimize the device structure and performance at various typical frequencies, in a self-consistent manner together with thermal and electronic limitations. The optimization is focused on a reliable (operating temperature lower than 500 K) and high negative resistance level device, based on dipolar-layer single transit mode. However, FECTED presents additional interesting capabilities. Because of its nonlinear behavior, FECTED is capable to operate as a self-mixer. Moreover the FECTED-oscillator fundamental operating frequency can be easily modified by means of a variation of the gate reverse-bias voltage. All these features can be ingeniously combined. Thus the second part of this paper is devoted to the theoretical feasibility of simple front-end FECTED-circuits for short-range pulsed and FM-CW millimeter-wave radars.

II. Modeling

The theoretical investigations have been performed by means of a general time-domain electronic circuit simulator [7]. The main program solves the circuit Kirchhoff equations at each time step. Our method relies on the nodal analysis in order to benefit of the systematic matrix–vector procedure implicit to the topological approach [8]. The main program is linked to a library including a time-domain electrical model for each type of circuit branch. These numerous models allow the determination of the instantaneous voltage–current characteristic in every branch. The originality of our simulator comes from the use of numerical physical macroscopic models as semiconductor device models. This particular approach is here justified by the

Manuscript received November 22, 1999; revised December 1, 2000.

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Publisher Item Identifier S 0018-9480(01)05062-1.

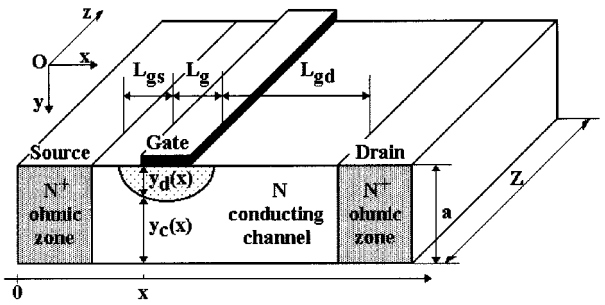

Fig. 1. Schematic illustration of an FECTED structure. Definition of geometrical quantities.

FECTED highly nonlinear dynamic behavior resulting from the strong interaction between the internal electric field and the free carriers in the device active zone. These spatio-temporal physical phenomena cannot be accurately described by means of simple analytical or lumped-element circuit based electrical models.

A. FECTED Modeling

The FECTED macroscopic physical model is a quasi-two-dimensional (Q-2-D) time-domain bipolar hydrodynamic model accounting for carrier energy relaxation effects. This kind of modeling is a good tradeoff between accuracy and computer efficiency. It allows the simulation of the whole semiconductor structure, including the ohmic zones, on long enough duration. The Q-2-D FECTED modeling relies on the basic assumption that, in the N-conducting channel, the electron and hole transport is one-dimensional (1-D) along the source–drain axis (x-axis, see Fig. 1). This means that the equipotential lines are perpendicular to the x-axis. This assumption has been validated by two-dimensional (2-D) FET modeling [9], [10]. The carrier transport 2-D effects mainly result from the reverse-biased gate Schottky contact. They are taken into account assuming that the space–charge zone due to the Schottky barrier is fully depleted. The local thickness of the depleted zone is calculated following Schockley's modeling [11]

$$y_d(x) = a\sqrt{\frac{|V_{\rm gs}| + V_b + V(x)}{V_p}} \tag{1}$$

where

- $y_d(x)$ thickness of the depleted zone at the x-location;
- a N-zone thickness;
- $V_{\rm gs}$ gate bias voltage;
- V_b Schottky barrier height;
- $V(x)$ electrostatic potential at the x-location;
- $V_p = a^2qN/2\varepsilon$ pinchoff voltage;
- q electronic charge;
- N doping level of the active zone;
- ε semiconductor permittivity.

A second 2-D effect results from the carrier parasitic conduction through the semiinsulating (SI) substrate. It is taken into account assuming a modified conductive channel thickness following Cappy's modeling [12]

$$y_c(x) = a - y_d(x) + y_s\left(\frac{n(x) - N(x)}{n(x)}\right), \quad \text{where } n(x) > N(x) \tag{2}$$

- $y_c(x)$ effective conductive channel thickness;
- $n(x)$ local free carrier density;
- y_s $= L_g/2$ carrier injection equivalent thickness.

Thus, the present FECTED modeling is based on the numerical solution of the electron and hole continuity, average total energy conservation, and Poisson's equations. These equations are modified to account for the x-variation of the cross section of the effective conducting channel as follows.

Continuity equations

$$\frac{\partial(ny_c)}{\partial t} = -\frac{\partial(nv_n y_c)}{\partial x} + (g-u)y_c \tag{3}$$

$$\frac{\partial(py_c)}{\partial t} = -\frac{\partial(pv_p y_c)}{\partial x} + (g-u)y_c. \tag{4}$$

Energy conservation equations

$$\frac{\partial\varepsilon_n}{\partial t} = -Ev_n - v_n\frac{\partial\varepsilon_n}{\partial x} - \frac{1}{n}\frac{\partial(nv_nkT_n)}{\partial x} - \frac{\varepsilon_n - \varepsilon_0}{\tau_{\varepsilon_n}} - \frac{\varepsilon_n}{n}(g-u) \tag{5}$$

$$\frac{\partial\varepsilon_p}{\partial t} = +Ev_p - v_p\frac{\partial\varepsilon_p}{\partial x} - \frac{1}{p}\frac{\partial(pv_pkT_p)}{\partial x} - \frac{\varepsilon_p - \varepsilon_0}{\tau_{\varepsilon_p}} - \frac{\varepsilon_p}{p}(g-u). \tag{6}$$

Poisson's equation

$$\frac{\partial(Ey_c)}{\partial x} = \frac{q}{\varepsilon}(p - n + N_d - N_a)y_c. \tag{7}$$

Current equations

$$i = Z\left(y_cJ_n + y_cJ_p + \varepsilon\frac{\partial(Ey_c)}{\partial t}\right) \tag{8}$$

$$J_n = -qnv_n = q\mu_n\left(nE + \frac{\partial nkT_n}{\partial x}\right) \tag{9}$$

$$J_p = qpv_p = q\mu_p\left(pE - \frac{\partial pkT_p}{\partial x}\right). \tag{10}$$

where n and p are the free electron and hole densities, respectively, E is the electric field, N_d and N_a are the donor and acceptor impurity concentrations, g is the impact ionization rate, u is the recombination rate, ε is the total average energy (expressed in electronvolts), ε_0 is the thermal energy (electronvolts), v is the average velocity, kT is the electronic temperature (expressed in electronvolts), τ_ε is the energy relaxation time, i is the total drain current, J is the conduction current density, and μ is the mobility. The subscripts n and p denote the quantities relative to electrons and holes, respectively.

Note that the depletion effects resulting from the surface potential are neglected. This assumption does not question the validity of this paper. To take this effect into account will yield a shift of the optimum geometrical values, especially the epitaxial layer thickness. The model does not presently take into account trapping effects. This means that we neglect phenomena such as drain and gate lag, which could affect the transient regime at low frequencies. Nevertheless, this does not question the feasibility of the millimeter-wave radar applications described below. Moreover, the device operation under

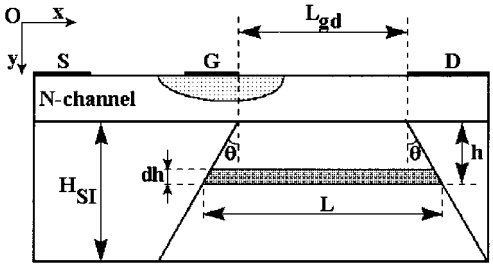

Fig. 2. FECTED thermal model.

forward-biased gate conditions cannot be presently modeled. These modified equations are solved by means of a linearized implicit finite-difference method [13]. In the particular case of FECTED simulations, numerical stability criteria impose a close to 10^{-15}-s temporal increment and a spatial increment of the order of 10^{-8} m. In this energy model, the electron and hole transport parameters, energy relaxation times, and electronic temperatures are considered as instantaneous functions of the carrier average energy [1]. Following Shur, the relevant quantities are deduced from Monte Carlo microscopic modeling under static steady-state conditions [14].

B. FECTED Thermal Modeling

The simplified FECTED thermal model relies on the determination of its equivalent thermal resistance, according to the following assumptions (see Fig. 2):

- most of the Joule power is dissipated in the gate–drain region;
- heat flux propagates orthogonally to the conduction current, namely, along the y-axis;
- convection and radiation effects are neglected;
- heat diffusion is uniform along the gatewidth (namely, the z-axis);
- heat diffusion profile in the (x, y) plane of the SI substrate is cone shaped.

The thermal resistance of an elementary cell $dv = LZdh$ located at a distance h from the interface between the SI substrate and N-channel is expressed as

$$dR_{\rm th} = \frac{1}{\sigma_{\rm th}} \frac{dh}{LZ}. \tag{11}$$

$\sigma_{\rm th}$ is the SI substrate thermal conductivity and $L = L_{\rm gd} + 2h(tg\theta)$.

Assuming that $H_{\rm SI}$ is the thickness of the SI substrate, the whole FECTED thermal resistance comes from

$$R_{\rm th} = \int_0^{H_{\rm SI}} dR_{\rm th} = \frac{1}{2\sigma_{\rm th} Z(tg\theta)} \ln\left[1 + \frac{2H_{\rm SI}}{L_{\rm gd}}(tg\theta)\right]. \tag{12}$$

We consider an isotropic heat diffusion in the (x, y) plane corresponding to $\theta = 45°$. Finally, the FECTED thermal resistance is given by

$$R_{\rm th} = \frac{1}{2Z\sigma_{\rm th}} \ln\left[1 + \frac{2H_{\rm SI}}{L_{\rm gd}}\right]. \tag{13}$$

Thus, for a given application (fixed $L_{\rm gd}$ and $\sigma_{\rm th}$ values), $R_{\rm th}$ is a decreasing function of the $H_{\rm SI}$ SI substrate thickness. The minimum $H_{\rm SI}$ value results from mechanical constraints. It has been estimated to be close to 100 μm. $R_{\rm th}$ is also inversely proportional to the transistor Z development. It comes from this feature that the device temperature rise ΔT does not depend on the Z gatewidth since $\Delta T = V_{\rm ds_0} J_{\rm ds_0} aZR_{\rm th}$. However, for a single gate–finger structure, the gatewidth maximum value is limited by the parasitic propagation effects along the gate contact. For a multifinger structure, the present thermal model remains valid following the assumption that the various heat diffusion profiles do not overlap.

III. FECTED Performance at Millimeter Wave

The potential performance of $Ga_{0.47}In_{0.53}As$ (lattice-matched to InP), GaAs, and InP millimeter-wave FECTED have been investigated. The comparative study has been focused on fixed operating frequencies related to typical applications, namely, 29–33–38–60–77–94 GHz. The optimization has been performed by means of continuous wave (CW) pure sine simulations ($V_{\rm ds}(t) = V_{\rm ds_0} + V_{\rm RF}\sin(\omega t)$) [15]. This simplified modeling relies on the assumption that the RF load circuit exhibits an ideal infinite Q-factor at the expected operating frequency. This kind of modeling is useful to investigate the device internal dynamics, its intrinsic RF-performance, impedance level, and dc-bias conditions. Thus, the device structure has been optimized, accounting in a consistent manner for thermal and electronic limitations (namely, maximum operating temperature and minimum load impedance, respectively), according to the following assumptions.

- Among the possible FECTED operating modes, we focus on the dipolar charge layer and single transit operating mode, namely, we limit our investigations to power generation at the fundamental transit frequency. This particular mode is achieved when the drain dc current is close to what we call the valley current, defined as $I_{\rm valley} = aZqNv_s$, where v_s is the electron saturation velocity.
- For safe operation, the FECTED operating temperature is kept lower than 500 K, accounting for a 20 °C external temperature (this operating temperature value is commonly accepted as the maximum temperature allowing a reliable operation).
- We choose a 50-Ω load resistance.

Systematic investigations have been performed to quantify the influence of each of the parameters determining the device performance. In this paper, we only give a brief summary of the main evolutions obtained. The results are illustrated here in the particular case of a 33-GHz GaAs device, noting that the main tendencies do not depend on the material considered among the three previously mentioned semiconductors. Next, self-consistent simulations have been performed to define the theoretically optimum structure for each frequency of interest. Here, we summarize the main results of this study.

A. Operating Mode

As a first theoretical result, Fig. 3 illustrates the FECTED dipolar charge layer and single transit operating mode. It shows

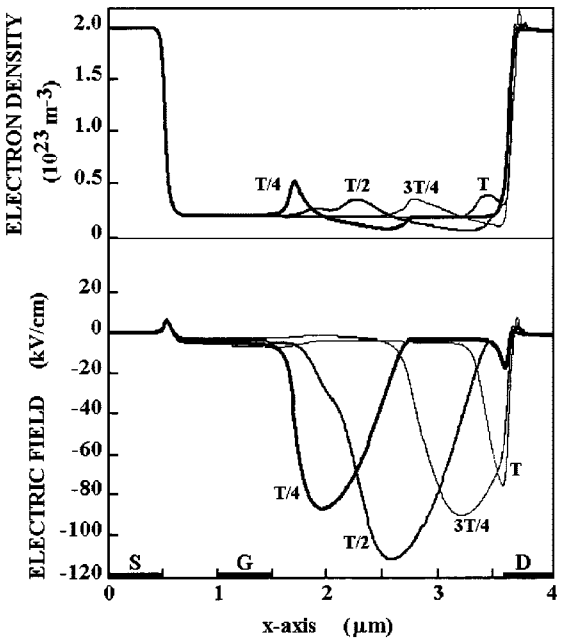

Fig. 3. Dipolar charge layer single transit operating mode: spatial evolutions of the free carrier density and electric field, every quarter of a 33-GHz cycle. GaAs—400 K: $V_{\mathrm{ds}_0} = 7$ V, $V_{\mathrm{RF}} = 4.2$ V, $V_{\mathrm{gs}_0} = 0$ V, $L_{\mathrm{gs}} = L_g = 0.5$ μm, $L_{\mathrm{gd}} = 2.1$ μm, $a = 0.8$ μm, $Z = 250$ μm, $N = 210^{22}$ m^{-3}, $I_{\mathrm{ds}_0} = 61$ mA, $I_{\mathrm{ds}_{\mathrm{rf}}} = 64$ mA.

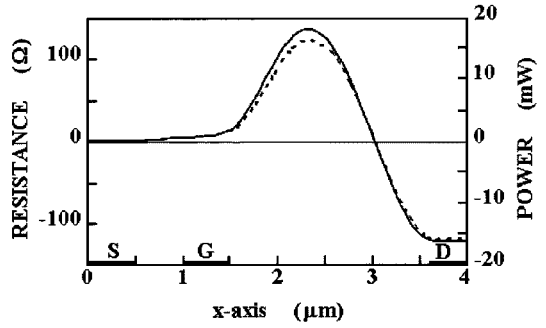

Fig. 4. Spatial evolution of the local RF resistance (solid line) and emitted RF power (dashed line) obtained by means of Fourier analysis of the local voltage and current waveforms for the device and operating mode described in Fig. 3.

the spatial evolutions of free electron density and electric field every quarter of a 33-GHz cycle in a GaAs structure. This figure clearly shows that the electron accumulation layer resulting from the intervalley transfer phenomenon is followed by a depleted zone. The whole constitutes the dipolar charge layer. This layer drifts under the action of the electric field toward the ohmic drain contact where it is collected at the end of the period. The local Fourier analysis of the voltage and current waveforms allows to characterize the average dynamic electrical behavior along the device. Fig. 4 shows the spatial evolution of the local RF resistance and emitted RF power. Here, we observe the typical behavior of this kind of operating mode [1], and especially the existence of a "dead zone," corresponding to the distance necessary for heating the carriers and yielding their intervalley transfer. Finally, the effective active zone corresponding to the charge instability nucleation and transit and, thus, RF-power generation, is roughly located in the gate–drain region.

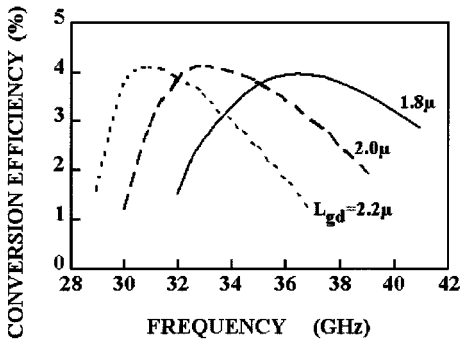

Fig. 5. DC to RF conversion efficiency versus frequency for various values of the gate–drain length. GaAs—400 K: $V_{\mathrm{ds}_0} = 7$ V, $V_{\mathrm{RF}} = 4.2$ V, $V_{\mathrm{gs}_0} = 0$ V, $L_{\mathrm{gs}} = L_g = 0.5$ μm, $a = 0.8$ μm, $Z = 250$ μm, $N = 210^{22}$ m^{-3}.

B. Gate–Drain Length

The optimum fundamental transit frequency f_0 can be estimated in a first approximation by the gate–drain length L_{gd} and the electron saturated velocity v_s as

$$f_0 = v_s / L_{\mathrm{gd}}. \tag{14}$$

Fig. 5 is an accurate illustration of the dependence between the FECTED dc to RF conversion efficiency and f_0 for various L_{gd} values. These results clearly point out the existence of an optimum operating frequency for each L_{gd} value.

C. Source–Gate and Gate Lengths

As previously mentioned, the source–gate zone behaves as a lossy RF resistance, the value of which depends on the $(L_{\mathrm{gs}} + L_g)$ value. The simulations demonstrate that the FECTED RF performance linearly decrease with the L_{gs} value. Indeed, in this kind of device, the intervalley transfer occurs at the end of the gate region due to the carrier velocity overshoot linked to the channel narrowing [12]. Thus, the source–gate region does not take part in the physical phenomena involved in the device operation. Consequently, the source–gate length must be as short as possible. However, its minimum value is practically limited by the source–gate parasitic coupling effects. A 0.5-μm value appears as a good tradeoff. RF losses also slightly increase with the L_g gatelength value. Once again, the minimum L_g value is limited. Indeed, a short gatelength value enhances the nonstationary effects occurring under the gate. This yields an increasing of the amplitude of the electron accumulation layer nucleated at the gate output. Especially in InP devices, this effect can be sufficiently pronounced to disturb the internal operating mode. A 0.5-μm L_g value seems to be a good tradeoff between the RF performance and the operating mode stability.

D. Channel Doping Level

From a general point-of-view, in such a transit time device, the emitted RF power and the negative resistance level are an increasing function of the active zone doping level. Unfortunately, the drain dc current and, consequently, the Joule dissipated power and operating temperature also increase with the doping level. Due to the maximum operating temperature imposed in our simulation, it then becomes necessary to decrease

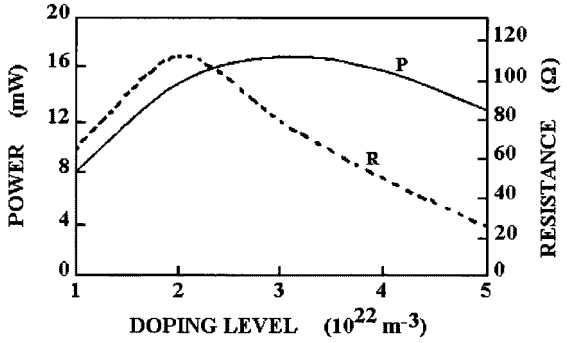

Fig. 6. Emitted RF power and modulus of the negative resistance level as a function of the channel doping level. GaAs—440 K: $f_0 = 35$ GHz, $V_{\rm RF}/V_{\rm ds_0} = 60\%$, $V_{\rm gs_0} = 0$ V, $L_{\rm gs} = L_g = 0.5$ μm, $L_{\rm gd} = 2$ μm, $a = 0.8$ μm, $Z = 250$ μm, $V_{\rm ds_0}$ is varied to ensure a constant operating temperature.

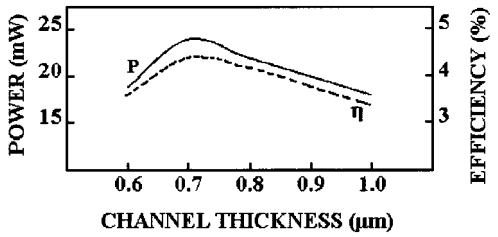

Fig. 7. Emitted RF power and conversion efficiency versus the N-channel thickness. GaAs—400 K: $f_0 = 33$ GHz, $V_{\rm RF}/V_{\rm ds_0} = 75\%$, $V_{\rm gs_0} = 0$ V, $L_{\rm gs} = L_g = 0.5$ μm, $L_{\rm gd} = 2$ μm, $N = 4\,10^{22}$ m^{-3}, $Z = 250$ μm, $V_{\rm ds_0}$ is varied to ensure a constant operating temperature.

the drain–source dc voltage in order to limit the temperature increasing. This yields a degradation of the operating mode, and a subsequent resistance level decreasing. This explains the evolutions illustrated in Fig. 6, where we have reported the evolutions of the emitted RF power and the associated negative resistance level versus the channel doping level. This figure points out an optimum doping-level value corresponding to a resistance peak and maximum RF power. Simulations also demonstrate that the optimum doping-level value is not the same for a device optimized for a maximum conversion efficiency or optimized for a maximum emitted RF power. We must also emphasize that the electric-field intensity at the NN^+ drain interface increases with the N doping level. This phenomenon yields a limitation due to the semiconductor avalanche breakdown threshold. This feature especially concerns GaInAs devices. Thus, their design has made the purpose of special care to avoid impact ionization carrier generation, accounting for available carrier transport data.

E. Channel Thickness

The N-epitaxial layer thickness (or channel thickness) does not fundamentally influence the carrier transit conditions and, consequently, the $L_{\rm gd}$ value. However, it determines the device RF operating-mode type. Accounting for the N active zone doping level considered here, and for a $V_{\rm gs_0} = 0$ V gate–source voltage, thickness values less than 0.5 μm lead to the FET operating mode [2]. On the opposite values higher than 1.5-μm lead to the accumulation layer and transit mode classically observed in millimeter-wave N^+NN^+ mesa Gunn diodes [16]. Thermally consistent simulations point out the existence of an optimum channel thickness in order to achieve the expected dipolar-layer mode. However, as can be seen from Fig. 7, this parameter is not too critical. Nevertheless, as it determines the device cross-sectional area, it must be chosen in accordance with the thermal and electronic limitations previously mentioned.

It must be emphasized that the channel thickness would never be disconnected from the gate–source voltage since this last parameter also allows to drive the operating mode by reducing the actual channel thickness under the gate. Namely, the FET mode can also be achieved, for a given epitaxial layer thickness, by increasing the reverse gate–source voltage. The results of the optimization study would be shifted if we choose to optimize the device for another gate–source voltage value, but this would not fundamentally change the qualitative description of the various operating modes. That is why the $I_{\rm valley}$ notion is concise—since it links the current, depending on the gate–source voltage, and the epitaxial layer thickness.

F. Gatewidth

We assume in our modeling that the FECTED internal operation does not depend on the z-direction and is, consequently, not influenced by the gate-development Z value. As previously mentioned, the operating temperature does not depend on the gatewidth. Nevertheless, this parameter determines the device cross-sectional area and, consequently, the RF-impedance level. Thus, the gatewidth is firstly determined by the minimum matchable impedance chosen. However, since the FECTED impedance level is naturally high, the Z value can easily reach relatively high values. Another limitation then appears, resulting from the parasitic propagation effects along the gate z-direction. Practically speaking, this involves the realization of multifinger devices. Here, we consider a gate–finger maximum length equal to one-tenth of the semiconductor material guided wavelength $\lambda_g = c/f_0\sqrt{\varepsilon_r}$, where c is the light velocity and ε_r is the semiconductor relative permittivity.

G. Main Results

The GaAs, $Ga_{0.47}In_{0.53}As$ and InP FECTED structure and performance have then been optimized at selected frequencies in a self-consistent manner, together with thermal and electronic limitations. In this study, several parameters remain constant whatever the material and the frequency may be: $H_{\rm SI} = 100$ μm, $L_{\rm gs} = 0.5$ μm. The gatelength value is not critical and has been chosen to be close to 0.5 μm. In all cases, the results are given for a 50-Ω negative resistance value at the considered frequency (it appeared that the device Q-factor lies between 1–2) and a $V_{\rm gs_0} = 0$ V value. Accounting for these parameters, the optimization study has been carried out up to a 500-K operating temperature in such a way that the best tradeoff between RF-power level and conversion efficiency value is found. It results from this exhaustive study that the optimum operating temperature lies in the 400–450-K range.

The results are summarized in Tables I–III, for GaAs, InP, and GaInAs devices, respectively. Note that GaInAs FECTED performance have been investigated for operating frequencies

TABLE I
GaAs DEVICES

GaAs FECTED				
F (GHz)	33	60	77	94
L_{gd} (μm)	2.0	0.9	0.7	0.5
$N(10^{22}\ \mathrm{m}^{-3})$	2	2	2	2
a (μm)	0.9	0.8	0.7	0.7
Z (μm)	4*250	5*125	6*100	6*80
P_{RF} (mW)	80	40	38	25
η_{RF} (%)	4.5	4.2	3.8	3.2

TABLE II
InP DEVICES

InP FECTED				
F (GHz)	33	60	77	94
L_{gd} (μm)	1.9	1.1	0.7	0.5
$N(10^{22}\ \mathrm{m}^{-3})$	2	2	3	4
a (μm)	0.7	0.7	0.8	0.7
Z (μm)	3*200	3*135	3*100	3*85
P_{RF} (mW)	234	85	30	24
η_{RF} (%)	14	7.4	4.6	3.5

TABLE III
GaInAs DEVICES

$Ga_{0.47}In_{0.53}As$ FECTED		
F (GHz)	29	38
L_{gd} (μm)	1.75	1.2
$N(10^{22}\ \mathrm{m}^{-3})$	4	4
a (μm)	0.8	0.8
Z (μm)	2*190	2*180
P_{RF} (mW)	240	216
η_{RF} (%)	18	16

lower than 40 GHz since the potential of this material strongly decreases for higher frequencies as compared to GaAs and InP materials [17]. The Z gatewidth is expressed here as a number of elementary gate fingers. Here, we find the classical comparison between these materials, namely, the superiority of InP devices over GaAs ones, and the fact that RF performance of GaAs devices are essentially electronically limited while RF performance of InP devices are rather thermally limited [18]. Note that the attractive results achieved for GaInAs devices correspond to a high doping-level value and, therefore, require a very high quality epitaxial layer because of impact ionization carrier generation problems.

IV. MILLIMETER-WAVE APPLICATIONS

FECTED applications are not limited to RF-power generation. Due to its nonlinear behavior, the FECTED can operate as a self-mixer when RF signals are applied across the gate and/or drain terminals. Moreover, the FECTED oscillator fundamental operating frequency can be easily controlled by means of the reverse gate voltage. These various capabilities can be ingeniously combined. Thus, we have theoretically investigated the feasibility of a simple FECTED front-end transmission/reception circuit for short-range millimeter-wave radar applications.

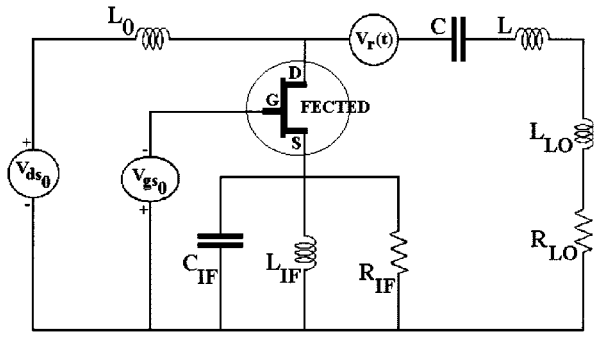

Fig. 8. FECTED-radar lumped-element equivalent circuit.

Time-domain modeling has been performed to simulate the successive phases of the FECTED-radar operation, namely, the transmission and reception phases, with and without obstacle detection, respectively. Fig. 8 depicts the radar equivalent circuit in which the FECTED is the lonely active semiconductor device. The drain dc-bias circuit is constituted of a V_{ds_0} voltage-generator series connected with an RF-signal decoupling inductance. The branch accounting for the FECTED–drain RF-load circuit represents the matched transmission/reception antenna. It consists of the following three series connected elements.

- The resonant LC circuit allows to insulate the drain dc-bias branch from the RF one. It also allows to modify the drain load circuit Q-factor.
- The $R_{\mathrm{LO}}L_{\mathrm{LO}}$ circuit matches the FECTED impedance at the fixed transmission operating frequency. The values of these elements are deduced from the pure sine modeling.
- An ideal voltage generator $V_r(t)$ symbolizes the echo signal received after the reflexion of the incident signal on the obstacle.

The $V_r(t)$ waveform is defined as the delayed and attenuated RF signal across the load resistance

$$V_r(t) = KV_{R_{\mathrm{LO}}}(t-\tau), \qquad \text{with} \quad K<1. \tag{15}$$

The instantaneous gate bias is provided by the $V_{\mathrm{gs}}(t)$ voltage generator. Thus, the radar operating mode can be varied from pulsed mode to requency-modulation continuous-wave (FM–CW) mode, for instance, by only modifying the $V_{\mathrm{gs}}(t)$ waveform.

The IF load circuit is located in the FECTED-source branch.

As an example, Fig. 9 illustrates the whole operating cycle of a 35-GHz GaAs FECTED front-end radar operating under pulsed regime. The results show the V_{gs} and V_r waveforms, the evolutions of the FECTED "instantaneous" fundamental frequency and the associated emitted RF-power level, and that of the drain current. Note that only the signal envelope of V_r and I_{ds} is visible because of the simulation duration (25 ns) and the corresponding high number of RF-signal periods.

The first phase, starting at $t = 1$ ns and lasting 10 ns, is the emission phase. It starts by a short transient resulting from the gate–bias variation from the -2-V value, corresponding to the reception phase of the previous operating cycle, to the

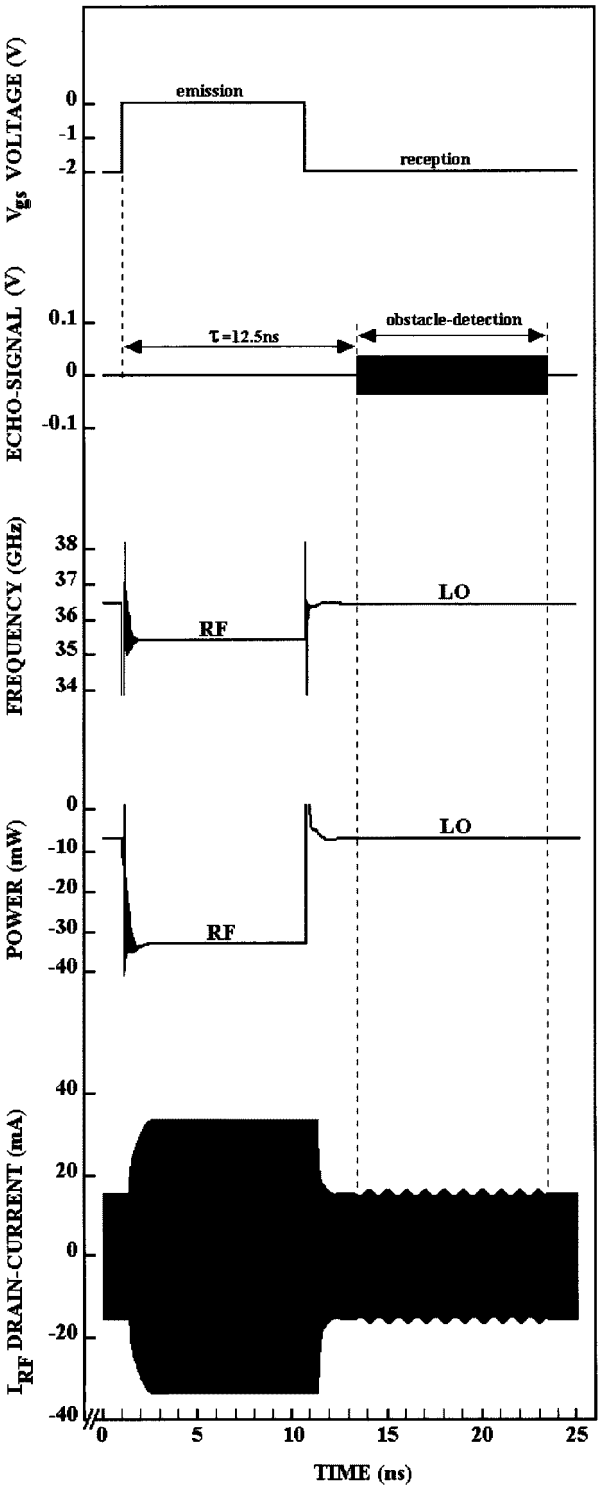

Fig. 9. Full cycle of a 35-GHz GaAs FECTED radar operated under pulsed mode. Temporal evolutions of the gate–source bias voltage, echo signal, "instantaneous" fundamental frequency, emitted RF power, and drain current.

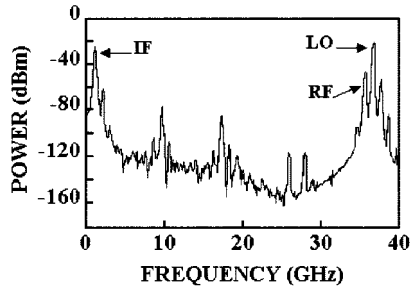

Fig. 10. Frequency spectrum of the power collected across the IF resistance during the obstacle-detection phase described in Fig. 9.

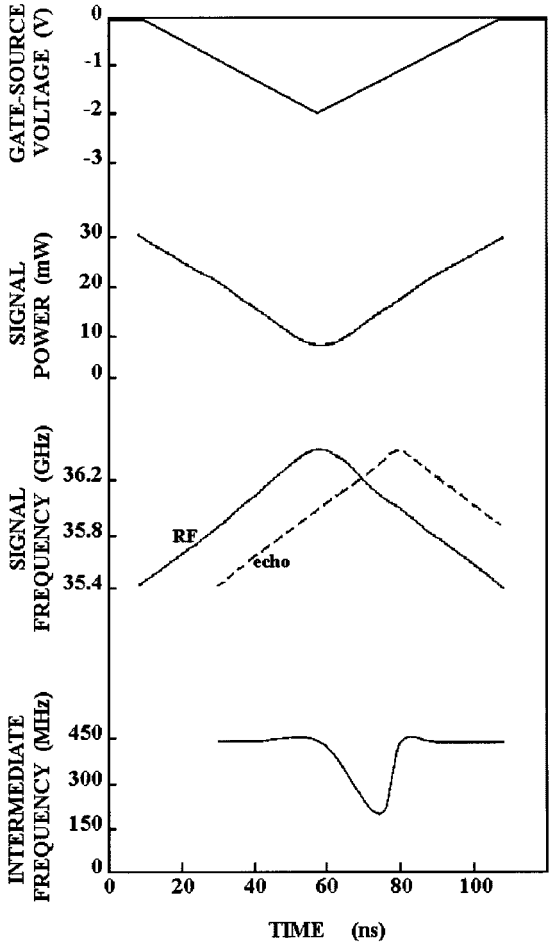

Fig. 11. Full cycle of a 35-GHz GaAs FECTED radar operated under an FM-CW mode. Temporal evolutions of the gate–source bias voltage, emitted RF-power, frequency of the RF and echo signals, and IF.

0-V value. Next, under steady-state operation, the transmitted RF-power level is of the order of $P_{\mathrm{RF}} = 35$ mW at a frequency close to $f_{\mathrm{RF}} = 35.5$ GHz. The reception phase beginning is imposed at $t = 11$ ns by means of the gate–bias variation from 0 to -2 V. In this phase, the FECTED-oscillator behaves as a local oscillator. The gate–bias variation yields a change of the fundamental operating frequency, which stabilizes around $f_{\mathrm{LO}} = 36.5$ GHz. The steady-state emitted power level is then close to $P_{\mathrm{LO}} = 8$ mW. The obstacle-detection phase starts at $t = 13.5$ ns. The results show that the reflected signal does not disturb the FECTED operation. We observe a low-frequency modulation of the drain current. This effect clearly points out the self-mixing operation. Moreover, Fig. 10 illustrates the frequency spectrum of the power collected across the IF resistance during the obstacle-detection phase. The IF line indicates the obstacle detection. The presence of the RF and

LO lines results from the IF-circuit imperfect filtering. Note that we have intentionally chosen a high IF (1 GHz), at first to simplify the result presentation, and then to limit the CPU time cost. A lower IF would yield a more realistic and usable operation with, e.g., lower P_{RF} to P_{LO} variations.

As a second example, Fig. 11 summarizes the whole operating cycle of the previous 35-GHz GaAs FECTED circuit now operating under an FM-CW regime. The gate–voltage waveform is, in this case, a 100-ns-period serrated signal. The $V_r(t)$ echo signal is achieved by memorizing the RF signal across the load resistance, and then applying a 22-ns delay and a 100-attenuation factor. This waveform allows to simulate the case of a motionless obstacle. The "instantaneous" frequency evolutions of the RF and echo signals show that the fundamental operating RF-frequency variation exhibits a good linearity versus the gate–bias voltage. This variation is here of the order of 500 MHz/V. This RF-frequency variation yields a strong variation of the emitted RF power. This effect results from the high amplitude of the serrated gate signal (2 V). As noted previously, these operating conditions have been chosen to qualitatively demonstrate the feasibility of FECTED-radar operation. The evolution of the IF-signal "instantaneous" fundamental frequency is consistent with the temporal evolution of the difference between the RF- and echo-signal frequencies. Thus, the IF is nearly constant from $t = 30$ ns to $t = 55$ ns and from $t = 85$ ns to $t = 110$ ns. This effect characterizes the detection of a motionless obstacle.

V. Conclusion

The potential of millimeter-wave GaAs, GaInAs, and InP FECTED oscillators has been theoretically investigated. The study has been performed by means of a time-domain electronic circuit simulator including a Q-2-D bipolar hydrodynamic FECTED model. The optimization has demonstrated that, despite the severe thermal and electronic constraints we have chosen, the FECTED exhibits interesting performance for medium power applications. We must emphasize that the choice of less rigorous constraints (mainly a lower minimum matchable impedance) or possibly the choice of a multitransit operating mode, could yield higher RF performance for some specific applications. Transient simulations have demonstrated that the combination of various FECTED electrical features could yield the realization of simple front-end circuits for millimeter-wave short-range radar applications.

To summarize, the FECTED interest can be attributed to the following:

- its planar structure compatible with the monolithic-microwave integrated-circuit (MMIC) technology and a relatively simple technological process;
- the intrinsic stability of the transferred-electron effect;
- the various control mechanisms resulting from the use of the no-power-consuming gate port:
  - thermal control $I_{\mathrm{ds}_0} = f(V_{\mathrm{gs}_0})$;
  - frequency control $f_0 = f(V_{\mathrm{gs}}(t))$;
  - direct and subharmonic injection locking;
- IF power gain resulting from the FECTED low-frequency amplification capabilities (still to be demonstrated);
- optronic applications [19].

Future work will be devoted to device and circuits realization and experiments.

References

[1] M. R. Friscourt, "Etude des dispositifs à transfert électronique pour la génération de puissance en gamme millimétrique," M.S. thesis, Univ. Lille 1, Lille, France, 1985.

[2] P. A. Rolland, A. Cappy, and M. R. Friscourt, "GaAs monolithic transferred-electron devices for millimeter wave applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, St. Louis, MO, June 3–7, 1985.

[3] G. Rieder, H. W. Thim, R. Kuch, and K. Lübke, "Numerical and experimental study of a GaAs transferred-electron device without transit-time limitation," *AEÜ*, no. 5/6, pp. 217–222, 1983.

[4] H. Scheiber, K. Lübke, D. Grützmacher, C. G. Diskus, and H. W. Thim, "Numerical and experimental study of a GaAs transferred-electron device without transit-time limitation," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 2093–2098, Dec. 1989.

[5] K. Lübke, H. Scheiber, and H. W. Thim, "A voltage tunable 35 GHz monolithic GaAs FECTED oscillator," *IEEE Microwave Guided Wave Lett.*, vol. 1, pp. 35–37, Feb. 1991.

[6] A. L. Springer, C. G. Diskus, K. Lübke, and H. W. Thim, "A 60 GHz MMIC-compatible TED-oscillators," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 114–116, Apr. 1995.

[7] C. Dalle, P. A. Rolland, and M. R. Friscourt, "Time-domain numerical modeling of microwave non linear circuits," *Int. J. Numer. Modeling*, vol. 5, pp. 41–52, Feb. 1992.

[8] L. O. Chua and P. H. Lin, *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*. Englewood Cliffs, NJ: Prentice-Hall, 1975.

[9] P. A. Sandborn, J. R. East, and G. I. Haddad, "Quasi-two-dimensional modeling of GaAs MESFET," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 985–991, May 1987.

[10] C. M. Snowden and R. R. Pantoja, "Quasitwo-dimensional MESFET simulations for CAD," *IEEE Trans. Electron Devices*, vol. 36, pp. 1564–1574, Sept. 1989.

[11] W. Schockley, "A unipolar field-effect transistor," *Proc. IRE*, vol. 40, pp. 1365–1376, Nov. 1952.

[12] A. Cappy, "Sur un nouveau mod\èle de transistor à effet de champ à grille submicronique," M.S. thesis, Univ. Lille 1, Lille, France, 1981.

[13] M. Reiser, "Large-scale numerical simulation in semiconductor device modeling," *Comput. Methods App. Mech. Eng.*, vol. 1, pp. 17–38, 1972.

[14] M. S. Shur, "Influence of nonuniform field distribution on frequency limits of GaAs field-effect transistors," *Electron. Lett.*, vol. 12, no. 23, pp. 615–616, 1976.

[15] B. Culshaw, R. A. Giblin, and P. A. Blakey, "Avalanche diode oscillator: I—Basic concepts," *Int. J. Electron.*, vol. 37, pp. 577–632, 1974.

[16] H. Kroemer, "Non-linear space–charge domain dynamics in a semiconductor with negative differential mobility," *IEEE Trans. Electron Devices*, vol. ED-13, pp. 27–40, Jan. 1970.

[17] P. A. Rolland, E. Constant, G. Salmer, and R. Fauquembergue, "Comparative frequency behavior of GaAs, InP and GaInAs transferred-electron devices. Derivation of a simple comparative criterion," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 341–343, Mar. 1981.

[18] ——, "Frequency limitation of GaAs transferred-electron devices: Influence of operating DC and RF field values," *Electron. Lett.*, vol. 15, no. 13, pp. 373–374, June 1979.

[19] F. Driouch, M. R. Friscourt, and C. Dalle, "FECTED oscillator optronic application feasibility," *Solid State Electron.*, vol. 44, no. 8, pp. 1455–1461, Aug. 2000.

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